an instruction memory for storing the sequence of 8-bit microprocessor instructions;

means for fetching each stored instruction in turn and for analyzing each instruction to determine whether an instruction corresponds either to a fixed and predefined operation or to a user defined operation;

means for generating an address corresponding to the location of a subroutine if an instruction corresponds to a user defined operation,

wherein, in the event that an instruction corresponds to a fixed and predefined operation, the instruction is passed to the central processing unit for execution and, in the event that an instruction corresponds to a user defined operation, a subroutine corresponding to the instruction is called using the generated address.

17. (New) A microprocessor system according to claim 16, wherein instructions corresponding to fixed and predefined operations are distinguished from instructions corresponding to user defined operations by a bit in a predefined bit position of the instruction code, and the means for analyzing each stored instruction is arranged to check for the presence of a bit in that bit position.

18. (New) A microprocessor system according to claim 16, wherein the microprocessor system comprises a data memory arranged in use to store code defining said subroutines.

19. (New) A microprocessor system according to claim 17, wherein said distinguishing bit is the most significant bit of the instruction code, and the generating means is arranged to shift the code to the left by one or more bits.

20. (New) A microprocessor system according to claim 19, and comprising a program counter register which is arranged to load the bit shifted instruction.

21. (New) A microprocessor system according to claim 18, wherein the instruction memory is arranged to hold 8-bit wide instructions, while the data memory is arranged to hold 32-bit data values.

22. (New) A microprocessor system according to claim 16, and comprising a hardware stack arranged in use to store a return address when a subroutine is entered, the return address pointing to the next instruction in the instruction memory when execution of the subroutine is completed.

23. (New) A microprocessor system according to claim 22, wherein the central processing unit, instruction memory, data memory, hardware stack, and program counter are all coupled to a common bus.

24. (New) A microprocessor system according to claim 23, wherein the central processing unit, instruction memory, data memory, hardware stack, program counter, and common bus are integrated onto a single chip.

25. (New) A microprocessor system according to claim 16, wherein the central processing unit contains an arithmetic logic unit and a data stack, and the top two elements of the data stack are connected to the inputs of the arithmetic logic unit and the output of the arithmetic logic unit is connected to an internal data bus.

26. (New) A microprocessor system according to claim 25, wherein the top three elements of the data stack contain special-purpose circuits, which enable the execution of seven primitive stack operations directly in hardware.

27. (New) A microprocessor system according to claim 16, and comprising means for recognizing a fast return instruction folded with a regular instruction, by utilizing circuitry which decodes the fast call bit in an 8-bit bytecode and another dedicated bit or bits in the 8-bit bytecode.

28. (New) A microprocessor system according to claim 27, wherein said other dedicated bit is the second most significant bit in the 8-bit bytecode.

29. (New) A microprocessor system according to claim 16, wherein said Virtual Machine bytecodes are Java bytecodes.

30. (New) A microprocessor system, consisting of a central processing unit, 8-bit wide instruction memory, 32-bit wide data memory and a hardware stack connected